Description

Read/write amplifier for a DRAM memory cell, and DRAM
5 **memory**

The present invention relates firstly to a read/write
amplifier for a DRAM memory cell in accordance with the
preamble of patent claim 1. Furthermore, the invention
10 relates to a DRAM memory in accordance with the
preamble of patent claim 10. Finally, the invention
also relates to a method for evaluating DRAM memory
cells of a DRAM memory.

15 DRAM memory cells (Dynamic Random Access Memory cells)
and memories represent an important type of memory for
storing digital information. A DRAM is a memory in
which, after specification of an address, data can be
stored and read out again under this address. In DRAM
20 memory   cells   and   memories,   respectively,   the
information is not stored as a switching state of a
circuit but rather as a quantity of charge on a
capacitance. Consequently, such a memory cell can be
formed with only a storage capacitor and a selection
25 transistor. Since every capacitor has leakage currents
and leakage currents also flow via the selection
transistor, the information in the DRAM memory cell is
continuously degraded. The information content of the
memory cell is therefore lost over time. In order to
30 avoid this, the contents of the memory cells are
periodically read out, the memory contents are
evaluated and the memory cell is written to anew. This
means   that   the   charge   contents   of   the   storage
capacitors are refreshed again, which is referred to as
35 "refresh".

DRAM memory cells are usually interconnected to form
memory cell arrays, a DRAM memory having one or a
plurality of such memory cell arrays. Each memory cell

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is connected, or wired, to the cell periphery via at
least one word line and a bit line, the word line(s)
and the bit line being routed via the memory cell and
being oriented at least substantially perpendicularly
5   to one another. Through activation of a specific word
line, all the memory cells connected thereto can, via
their bit lines, be read, written to or refreshed with
regard to their information content.

10 In DRAM memory cells, digital information items can be
stored for example in the form of logic "0" and "1".
Each of these logic information items is assigned a
specific voltage value. By way of example, the voltage
value for logic "0" may be zero volts, while the
15 voltage value for logic "1" is 2 volts, for example.
Before the memory cells are read, a reference voltage,
for example a voltage of 1 volt is applied to all the
bit lines. During the reading of the memory cell, the
voltage value will either increase somewhat or else
20 decrease, depending on the information content of the
memory cell. This voltage change is compared with a
reference voltage prevailing on a reference bit line.
In this case, the reference bit line is connected to a
memory cell which is currently not being evaluated. If
25 the voltage value on the bit line that is to be
evaluated is higher than the reference voltage, the
information content logic "1" had been written to the
memory cell. In the case of smaller voltage values, the
information logic "0" had been written to the memory
30 cell. The voltage signal read from the bit line to be
evaluated and the reference bit line is conditioned and
processed further, for example amplified, in a
read/write amplifier.

35 Depending on the memory architecture, the bit lines
(BL) of the memory cells to be evaluated and the
respective reference bit lines (BBL) may be arranged
beside one another in one and the same memory cell

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array and thus form a bit line pair in each case. In
other memory architectures, the reference bit lines are
each situated in a different memory cell array.

5   As has already been mentioned, the logic information
     items "0" and "1" are stored in the form of charge in
     cell capacitances in the case of a DRAM memory. These
     charges are converted into a small voltage signal in a
     first section of the evaluation. The read/write
10   amplifier circuit of a DRAM memory has the task of
     amplifying this voltage signal to a full level. The
     amplified signal serves, on the one hand, for writing
     back the information that was destroyed in the memory
     cell during read-out, and, on the other hand, for
15   forwarding the information read to the DRAM periphery.
     The read/write amplifier circuit must perform the
     aforementioned tasks with high evaluation reliability
     and speed in conjunction with the smallest possible
     space requirement.

20

     Conventional read/write amplifier circuits generally
     comprise a number of components for assessing,
     amplifying and forwarding voltage signals read from the
     bit lines and reference bit lines.

25

     These components include, for example, at least one
     "N latch circuit" (NL), which serves for producing the
     low level for the voltage value. The N latch circuit
     has the task of amplifying a voltage signal to this low
30   level. With reference to the numerical example
     mentioned further above the low level might be, for
     example, the "0" volts value.

     Furthermore, the read/write amplifier may have at least
35   one "P latch circuit" (PL), which serves for producing
     a high level. Thus, the P latch circuit serves for
     amplifying a voltage signal to this high level, which

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corresponds to the "2" volts value, for example, in
connection with the numerical example mentioned above.

5   A further component for the read/write amplifier is,
for example, the "equalizer" (EQ), which serves for
producing a reference voltage value (precharge level)
on the bit lines.

Furthermore, the read/write amplifier may have at least
10   one "bit switch" (BS), which is used for connecting a
bit line pair - selected for example by a "column
address" - to external data lines.

Finally, the read/write amplifier may have one or more
15   transistors for changing over between different bit
lines. Such transistors are, for example, selection
transistors (MUX) for multiplexing the read/write
amplifiers between different bit line pairs.

20   The individual components of the read/write amplifier
will be explained in more detail in the further course
of the description.

Figure 1 diagrammatically illustrates a DRAM memory
25   which is known from the prior art and in which
different read/write amplifier circuits (SA) are
utilized for bit line pairs of adjacent memory cell
arrays (Arrays). Such read/write amplifier circuits are
also referred to as "shared sense amplifier". An
30   arrangement of the different read/write amplifier
circuits as illustrated in Figure 1 already leads to a
favorable ratio of the area proportions of memory cells
and read/write amplifier circuits.

35   Depending on the DRAM memory type, the area required by
the read/write amplifier circuit(s) can vary greatly in
relation to the total area of the memory. The absolute
area of a read/write amplifier circuit usually remains

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the same, so that the relative size of the read/write
amplifier circuit in the overall memory changes
depending on the memory architecture. In this case, the
relative size of the read/write amplifier circuits in a

5 DRAM memory may be between 5% and 30% of the total
memory area. There is, therefore, a need to minimize
the required area of the read/write amplifier circuits
as well as possible.

10 In a known DRAM memory, with the aid of a second metal
plane in the integrated circuit per memory cell array,
it is possible to evaluate an additional bit line pair
with each read/write amplifier circuit. This
architecture thus halves the required number of

15 read/write amplifier circuits in comparison with a
conventional memory architecture as described above.
However, the use of two metal planes is very cost-
intensive and hence disadvantageous.

20 Another approach which is known from the prior art and
serves for saving read/write amplifier area consists in
the multiple use of the same read/write amplifier for
different bit line pairs by multiplexing. Such an
approach is illustrated for example in Figure 2 and is

25 explained in more detail in the context of the
description of the figures. This known principle is
based on the multiple utilization of read/write
amplifier circuits for bit line pairs in the same
memory cell array. The read/write amplifier (SA) is

30 connected by selection transistors (MUX) to
respectively complementary halves of bit line pairs of
a cell array. The connected bit line pairs can be
evaluated in a customary manner. An unamplified voltage
signal develops on the unconnected bit line pairs. The

35 voltage signal must remain undisturbed until the
read/write amplifier circuit is changed over to the
corresponding bit lines. The signal amplification and
the writing back to the memory cells can then take

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place. During this second phase, the amplified voltage
levels must remain on the bit lines evaluated in the
first step. If the aforementioned preconditions are
met, then at the end of the second phase the read-out
5   information items of the entire cell array are written
back and the word line can be deactivated.

One disadvantage of this solution approach, however,
resides in the expected high degree of interference
10 with the voltage signal on the unconnected bit lines as
a result of capacitive overcoupling of the voltage
changes on the adjacent bit lines which are connected
to the read/write amplifier circuits. This interference
can become so great that the voltage changes caused
15 thereby no longer permit error-free evaluation of the
memory cells.

Furthermore US 4,916,667 discloses a DRAM memory in
which an equalize component is assigned to a first bit
20 line pair and the bit switch component is assigned to a
second bit line pair, in which case the first bit line
pair and the second bit line pair can be
interconnected.

25 US 5,757,692 describes a further semiconductor memory.

Taking the abovementioned prior art as a departure
point, the present invention is based on the object of
providing a read/write amplifier, a DRAM memory and
30 also a method for evaluating DRAM memory cells of a
DRAM memory with which the abovementioned disadvantages
are avoided. In particular, the intention is that the
read/write amplifier circuit can perform the tasks
intended for it with high evaluation reliability and
35 speed in conjunction with the smallest possible space
requirement.

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This object is achieved by means of the read/write
amplifier for a DRAM memory cell in accordance with
patent claim 1, the DRAM memory in accordance with
patent claim 10 and also the method for evaluating DRAM
5   memory cells of a DRAM memory in accordance with patent
claim 15. Further advantageous features, aspects and
details of the invention emerge from the dependent
claims, the description and the drawings. Advantages
and features which are described with regard to the
10 read/write amplifier likewise apply to the DRAM memory
and also the method. Advantages and features which are
described with regard to the DRAM memory likewise apply
to the read/write amplifier according to the invention
and also the method according to the invention. The
15 same applies analogously to the method according to the
invention.

The first aspect of the present invention provides a
read/write amplifier for a DRAM memory cell, which, for
20 evaluation of the information content of at least one
DRAM memory cell, is connected or can be connected to
at least one bit line and to at least one reference bit
line, which in each case form a bit line pair. The
read/write amplifier has a number of components for
25 assessment, amplification and forwarding of voltage
signals read from the bit lines and reference bit
lines. According to the invention, this read/write
amplifier is characterized in that it has a first
read/write amplifier element and a second read/write
30 amplifier element separate therefrom, and in that the
individual amplifier components are divided between the
two read/write amplifier elements.

This produces an area-optimized DRAM read/write
35 amplifier circuit which has only a small space
requirement and with which the evaluation of DRAM
memory cells, in particular of memory cells of a single

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memory cell array, can be evaluated with high
reliability and speed.

The read/write amplifier according to the invention
5   makes it possible to avoid the problems outlined with
respect to the prior art on account of the fact that
the individual components of the read/write amplifier
can be used for a plurality of bit line pairs in a
memory cell array and with simultaneous direct
10 amplification of all the signals being made possible.

A basic concept of the present invention is that the
individual components of the read/write amplifier
circuit are now divided between two read/write
15 amplifier elements. These two read/write amplifier
elements are embodied separately from one another. The
first read/write amplifier element (SAINT) serves
primarily for writing back cell information items,
while the second read/write amplifier element (SAEX)
20 can additionally drive the information item read out,
or the datum read out, into an external area of the
DRAM memory and enables the writing of cell information
items.

25 Since a plurality of bit lines, or bit line pairs, can
now be evaluated by one and the same read/write
amplifier which has merely been divided between two
amplifier elements, the requisite space requirement for
the read/write amplifier circuits in the entire DRAM
30 memory can be considerably reduced.

In the light of the present invention, evaluation of a
memory cell is understood to be not only the reading of
information items from a memory cell but also the
35 forwarding of the information and also the subsequent
writing back of the cell information at the end of the
evaluation operation.

For the mode of operation of the read/write amplifier
according to the invention, reference is likewise made
to the explanations regarding the method according to
the invention.

5

The amplifier components may advantageously have at
least one N latch circuit for amplifying a voltage
signal to a low level and/or at least one P latch
circuit for amplifying a voltage signal to a high level
10 and/or at least one equalizer for producing a reference
voltage value on the bit line(s) and the reference bit
line(s) and/or at least one bit switch for connecting
at least one selected bit line pair to at least one
external data line.

15

Preferably, at least one N latch circuit and at least
one P latch circuit may be provided in the first
read/write amplifier element.

20 Furthermore, the first read/write amplifier element may
be provided with at least one equalizer. The function
of the equalizer is to set the voltage signals
amplified to low levels and/or high levels after the
evaluation operation once again to the reference
25 voltage value.

At least one N latch circuit may advantageously be
provided in the second read/write amplifier element.

30 Furthermore, at least one bit switch may be provided in
the second read/write amplifier element. If only the
second read/write amplifier element is provided with a
bit switch, in each case only half of the memory cells
activated by a word line can potentially be read or
35 written to anew. In this case, the bit switch has the
following basic function. If a specific memory cell is
intended to be read, the entire page, that is to say
the quantity of all the memory cells which are

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connected to a word line, is addressed in which said
memory cell is situated. This means that the
information items of the entire page are read out. By
means of activation of the bit switch, that/those
5 memory cell(s) whose information content is actually of
interest can now be selected from the entire quantity
of the memory cells read.

In a further refinement, it is possible that the second
10 read/write amplifier element is connected or can be
connected to at least one external data line. These
external data lines lead from the evaluated DRAM memory
cell, or the memory cell array, through to the DRAM
memory periphery.
15

It is advantageously possible that the second
read/write amplifier element is connected or can be
connected to at least one further read/write amplifier.
This additional read/write amplifier, also called
20 "Secondary Sense Amplifier (SSA)" can further amplify
the voltage signals that have been read from the
read/write amplifier assigned to the DRAM memory and
have been correspondingly amplified, with the result
that these voltage signals can also be utilized further
25 outside the DRAM memory.

The first and/or the second read/write amplifier
element may have one or more transistors for changing
over between different bit lines and reference bit
30 lines, respectively. These transistors, which, for
example, are also called selection transistors or
multiplex transistors, determine which bit line pair is
actively connected to the first and/or second
read/write amplifier element.
35

A second aspect of the present invention provides a
DRAM memory, having a number of DRAM memory cells,
which each form one or more memory cell arrays, each

memory cell being connected to a bit line and the bit
lines furthermore being connected to at least one
read/write amplifier. The invention provides for the at
least one read/write amplifier to be designed as a
5   read/write amplifier according to the invention as
described above.

A DRAM memory according to the invention, designed in
this way, makes it possible for the individual memory
10 cells to be evaluated with high evaluation reliability
and speed in conjunction with a very small space
requirement of the read/write amplifier circuits and
hence of the DRAM memory. For the mode of operation of
the DRAM memory according to the invention, reference
15 is likewise made to the explanations concerning the
method according to the invention.

At least one word line may advantageously be provided,
which is routed across the memory cell array(s) of the
20 DRAM memory and, for activation of the DRAM memory
cells, is connected to one or more memory cell(s). In
this case, the at least one physical word line can be
divided by the selection transistors into two logical
word lines. The cell signals of one word line half are
25 amplified by the first read/write amplifier element,
while the cell signals of the other word line half are
amplified by the second read/write amplifier element.

Preferably, a plurality of bit lines of a memory cell
30 array are connected to the read/write amplifier.

In each case a bit line of a DRAM memory cell that is
to be evaluated and a reference bit line of a DRAM
memory cell that is not to be evaluated may form a bit
35 line pair, each bit line pair being connected both to
the first and to the second read/write amplifier
element.

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It may be the case here that the connection of a bit line and/or reference bit line to the read/write amplifier is activated or can be activated preferably via one or more transistors.

A third aspect of the present invention provides a method for evaluating DRAM memory cells of a DRAM memory, in particular of a DRAM memory according to the invention as described above, and in particular using a read/write amplifier according to the invention as described above, which method has the following steps.

Firstly, one or a plurality of memory cell(s) to be evaluated is/are activated via at least one word line. If a plurality of memory cells are intended to be evaluated, they are preferably situated within a single memory cell array. The memory cells connected to the word line can be read through the activation of said word line.

Afterward, the connection of at least one first bit line pair, formed from a bit line of the memory cell that is to be evaluated and a reference bit line of a memory cell that is not to be evaluated, to a first read/write amplifier element is activated and, at the same time, the connection of at least one second bit line pair, adjacent to the first bit line pair, to a second read/write amplifier element is activated, the two bit line pairs in each case being connected to the first and second read/write amplifier elements.

If the read/write amplifier is connected for example to two bit line pairs, that is to say each of the two read/write amplifier elements is in each case connected to both bit line pairs, the transistors may initially be switched in such a way that one of the two bit line pairs is actively coupled to the first read/write amplifier element, while the other bit line pair is

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actively coupled to the second read/write amplifier
element.

The voltage signals read out via the first bit line
5 pair are subsequently amplified by means of at least
one N latch circuit provided in the first read/write
amplifier element and also a P latch circuit. At the
same time, the voltage signals read out via the second
bit line pair are amplified by means of at least one N
10 latch circuit provided in the second read/write
amplifier element. This is done, for example, as
follows.

At the beginning of the evaluation, a reference voltage
15 is applied preferably to all of the bit lines. If the
cells to be read are activated, the voltage value
present on the bit line to be evaluated changes as a
result of the activation. By way of example, the
voltage value rises slightly in the case of an
20 information item of logic '1' situated in the memory
cell whereas it falls slightly in the case of a logic
information item "0" stored in the memory cell. In the
case of the unactivated reference bit line, however,
the voltage value remains substantially constant. By
25 comparison between the bit line (BL) and the reference
bit line (BBL), it is now possible to see what
information had been stored in the memory cell,
depending on whether the voltage value read out lies
above or below the reference voltage value.
30

The cell signals of the memory cells connected to the
second read/write amplifier element, or the voltage
values read out via the corresponding bit lines, are
initially amplified only by means of an N latch
35 circuit. If an information item logic "0" had been
stored in the memory cell to be evaluated, this means
that the voltage value present on the bit line to be
read at the beginning of the evaluation is less than

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the reference voltage value on the reference bit line.
The N latch circuit amplifies to the low level the
voltage values of those bit lines which have a lower
voltage value. In this case, this means that the memory
5   cell having the information item logic "0" is amplified
down to the low level. The voltage signal of the
reference bit line initially remains substantially
unchanged, or falls significantly less than the voltage
signal of the bit line.

10

If an information item logic "1" had been situated in
the memory cell to be evaluated, this would have led to
a slight voltage increase relative to the reference
voltage value. The N latch circuit would once again
15 have amplified the lower of the two voltage values down
to a low level. In this case, this would have been the
voltage value on the reference bit line. From the
substantially unchanging voltage value, or voltage
value falling to a significantly lesser degree, of the
20 bit line to be evaluated, it would then have been
possible to infer that the information content stored
in the memory cell to be evaluated is logic "1".

Also by using only a single N latch circuit in the
25 second read/write amplifier element, it is possible,
during the first amplification step, to state exactly
what kind of information item had been stored, or is
stored, in the memory cells. If the voltage value on
the bit line to be evaluated is pulled down to a low
30 level, it is known that the information in the memory
cell was logic "0". However, if the voltage value of
the reference bit line is pulled down to a low level,
it is known that the information in the memory cell was
logic "1".

35

At the same time as the amplification in the second
read/write amplifier element, the memory cells
connected to the first read/write amplifier element are

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also evaluated. In addition to the N latch circuit,
however, the first read/write amplifier element also
has a further P latch circuit. As has been described
above with regard to the second read/write amplifier

5 element, the respective lower voltages in a bit line
pair are amplified to the low level. The respective
other cell signals, that is to say the higher voltage
signals, are amplified to the full high level by means
of the P latch circuit. This means that if the voltage

10 value on the bit line of the memory cell to be
evaluated has been amplified down to a low level, the
voltage value present on the reference bit line is
amplified to the high level.

15 In principle, voltage signals amplified to both levels
are required in order to be able subsequently to write
back to the memory cells. This means that the voltage
values initially not amplified to high levels in the
second read/write amplifier element also still have to

20 be amplified in a corresponding manner.

After the voltage signals have been amplified in the
above way, the data of the memory cell(s) that is/are
to be evaluated and is/are actively connected to the

25 first read/write amplifier element are evaluated and
subsequently written back. After the writing back of
the data by the first read/write amplifier element, the
corresponding bit line pairs can be disconnected by the
selection transistors, with the result that they float

30 at full voltage levels.

The connection between the bit line pairs and the first
read/write amplifier element is subsequently changed
over in such a way that the P latch circuit of the

35 first read/write amplifier element is now changed over
to the second read/write amplifier element.

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The N latch circuit of the first read/write amplifier
element is then switched off, while the still active P
latch circuit is coupled to the bit line pair connected
to the second read/write amplifier element. As a
5 result, the voltages of the bit line pair that have
hitherto not been amplified to high levels can be
amplified to a full level. In this case, the N latch
circuit of the second read/write amplifier element is
likewise held active.
10

The data of the memory cell(s) that is/are to be
evaluated and is/are actively connected to the second
read/write amplifier element are subsequently evaluated
and written back.
15

Afterward, in order to end the evaluation method, the
memory cells that are to be evaluated can be
deactivated.

20 There is no loss of time caused by the successive
amplification to the high level of the individual bit
line pairs by only a single P latch circuit, since the
cell information items can already be output to the
outside via the second read/write amplifier element
25 before both levels, that is to say the low level and
also the high level, are fully installed.

Before the evaluation of the memory cells, a uniform
reference voltage can be applied to all the bit lines
30 of the memory cells provided in one or more memory cell
arrays. The generation and the function of such a
reference voltage have been thoroughly explained
further above.

35 Preferably, after the activation of a bit switch
provided in the second read/write amplifier element, a
voltage difference can be generated on one or more
external data line(s) connected to said bit switch.

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This voltage difference can then be evaluated by a further, external read/write amplifier.

5 After the end of the evaluation operation, the uniform reference voltage may advantageously be applied to all the bit lines of the evaluated memory cells via an equalizer.

10 The invention will now be explained in more detail using exemplary embodiments with reference to the accompanying drawing, in which:

Figure 1 shows a circuit arrangement of a DRAM memory known from the prior art;

15 Figure 2 shows a circuit arrangement of a further DRAM memory known from the prior art;

Figure 3 shows a circuit arrangement of a DRAM memory according to the present invention;

Figure 4 shows the signal sequence of the read/write
20 amplifier driving of a read/write amplifier according to the invention;

Figures 5a to 5c show voltage profiles for the internal read-out and writing back of different cell information items to memory cells connected by an active word line
25 and two bit lines; and

Figures 6a and 6b show voltage profiles for the external reading and writing of cell information items of a memory cell connected to a bit line.

30 Figure 1 illustrates a DRAM memory 10 which is known from the prior art and has a number of memory cell arrays 11. Three such memory cell arrays 11 (Arrays 1 to 3) are illustrated in the present exemplary embodiment. Each memory cell array 11 is provided with
35 a number of DRAM memory cells. Each DRAM memory cell is connected to a read/write amplifier (SA) 20 via a bit line 12. Each of the read/write amplifiers 20 is furthermore connected to a reference bit line 13.

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As can be seen from Figure 1, a read/write amplifier
circuit 20 is used in each case for bit line pairs 12,
13 of adjacent cell arrays 11, thereby already
5 obtaining a favorable ratio of the area proportions of
memory cells and read/write amplifier circuits 20.

Each of the read/write amplifiers 20 is provided with a
number of amplifier components. These amplifier
10 components are, for example, an N latch circuit (NL) 21
for amplifying a voltage signal to a low level, a P
latch circuit (PL) 22 for amplifying a voltage signal
to a high level, an equalizer (EQ) 23 for producing a
reference voltage value on the bit line(s) 12 and the
15 reference bit line(s) 13, and also a bit switch (BS) 24
for connecting at least one selected bit line pair 12,
13 to at least one external data line. In order to be
able to change over between different bit lines 12 and
reference bit lines 13, respectively, one or more
20 selection transistors (MUX) are furthermore provided
per read/write amplifier 20.

In the DRAM memory cells, digital information items can
be stored for example in the form of logic "0" and "1".
25 Each of these logic information items is assigned a
specific voltage value. By way of example, the voltage
value for logic "0" may be zero volts, while the
voltage value for logic "1" is 2 volts, for example.
Before the memory cell is read, a reference voltage,
30 for example a voltage of 1 volt, is applied to all the
bit lines 12 and reference bit lines 13. During the
reading of the memory cell, the voltage value on the
corresponding bit line 12 will either increase somewhat
or else decrease somewhat, depending on the information
35 content of the memory cell. This voltage change is
compared with the unchanged reference voltage still
prevailing on the reference bit line 13. If the voltage
value on the bit line 12 that is to be evaluated is

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higher than on the reference bit line 13, the
information content logic "1" had been written to the
memory cell. In the case of smaller voltage values, the
information item logic "0" had been written to the
5   memory cell. The voltage signals read from the bit line
12 to be evaluated and the reference bit line 13 are
conditioned and amplified by the read/write amplifier
20.

10 The DRAM memory 10 illustrated in Figure 2 is likewise
a memory architecture known from the prior art. The
DRAM memory 10 is provided with one or more memory cell
array(s) 11, in which a number of DRAM memory elements
15 are provided. For the sake of better clarity, only a
15 single memory cell array 11 is illustrated in Figure 2.
The individual memory cells 15 are represented by large
black dots. In order to be able to activate the
individual memory cells 15 a word line 14 is provided,
which is connected to a plurality of memory cells 15.
20 All the memory cells 15 connected to the word line 14
are activated by means of activation of said word line.

Furthermore, a number of bit lines 12 and reference bit
lines 13 are provided in each case, a bit line 12 and a
25 reference bit line 13 adjacent thereto in each case
forming a bit line pair 16. The association of a bit
line 12 and a reference bit line 13 as bit line pair 16
is symbolized in Figure 2 by a circle surrounding the
two bit lines 12, 13.
30

The DRAM memory 10 in accordance with Figure 2 has two
read/write amplifiers 20, where each read/write
amplifier 20 can be used for different bit line pairs
16 within the same memory cell array 11. Each
35 read/write amplifier 20 once again has an N latch
circuit 21, a P latch circuit 22, an equalizer 23 and
also a bit switch 24.

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The read/write amplifiers 20 are connected via
selection transistors (MUX1, MUX2) 25 to respectively
complementary halves of bit line pairs 16 of a memory
cell array 11. The connected bit line pairs 16 can be
5   evaluated in a customary manner. The unamplified
voltage signal develops on the unconnected bit line
pairs 16. The voltage signal must remain undisturbed
until the read/write amplifiers 20 are changed over to
the corresponding bit lines 12, 13 by means of
10 corresponding driving of the transistors 25. The signal
amplification and also the writing back to the memory
cells 15 can then take place. During this second phase,
the amplified voltage levels must remain on the bit
lines 12 evaluated in the first step.
15

As was explained in the context of the introduction to
the description, such a configuration of the DRAM
memory 10 has considerable disadvantages, however,
since the voltage signals on the unconnected bit lines
20 12, 13 are disturbed by capacitive overcoupling of the
voltage changes on the adjacent bit lines 12, 13 which
are connected to the read/write amplifiers 20.

A read/write amplifier circuit 20 according to the
25 invention, which enables DRAM memory cells to be
evaluated with high evaluation reliability and speed
and which has only a small space requirement, is
illustrated in connection with Figure 3.

30 Figure 3 illustrates a DRAM memory 10 having one or
more memory cell array(s) 11 having a number of DRAM
memory cells 15, some of the memory cells 15 once again
being represented as thick black dots and, for the sake
of better clarity, only a single memory cell array 11
35 being shown. The memory cells 15 of the memory cell
array (Cell Array) 11 are connected to a read/write
amplifier 30 via bit lines 12 and reference bit lines
13, respectively.

According to the invention, the read/write amplifier 30
has a first read/write amplifier element 40 and a
second read/write amplifier element 50 separate
5   therefrom. The individual amplifier components are
divided between the two read/write amplifier elements
40, 50.

The first read/write amplifier element (SAINT) 40 is
10 provided with an N latch circuit (NL) 41, a P latch
circuit (PL) 42 and also an equalizer (EQ) 43. The
individual amplifier components are connected via
selection transistors (MUX1, MUX2) 45 to bit lines (BL)
12 of memory cells 15 that are to be evaluated and also
15 reference bit lines (BBL) 13 of memory cells 15 that
are in each case not to be evaluated. A bit line 12 and
a reference bit line 13 in each case form a bit line
pair 16, which is once again symbolized by a circle
surrounding the corresponding bit lines. It is possible
20 to switch back and forth between different bit lines 12
and reference bit lines 13, respectively, by means of
corresponding driving of the selection transistors 45.

The individual bit lines 12 and reference bit lines 13
25 are likewise connected to the second read/write
amplifier element 50. The latter has an N latch circuit
(NLEX) 51 and also a bit switch (BS) 54. The individual
amplifier components are connected via corresponding
selection transistors (MUXEX1, MUXEX2) to the bit lines
30 12 and reference bit lines 13, respectively, with the
result that it is possible to switch back and forth
between individual bit lines 12 and, respectively,
reference bit lines 13 (and hence bit line pairs 16) by
means of corresponding driving.
35
The second read/write amplifier element 50 is connected
via at least one external data line 31 to a second

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read/write amplifier (SSA) 32, which is an external
read/write amplifier.

For the activation of the memory cells 15, the latter
5   are connected to a corresponding word line (WL) 14.

The mode of operation of such a DRAM memory 10 is now
described below.

10   In the exemplary embodiment illustrated in Figure 3,
the read/write amplifier element 40 serves primarily
for writing back the cell information, while the
read/write amplifier element 50 can additionally drive
the information read to the further read/write
15   amplifier 32 and enables the writing of cell
information items.

At the beginning of the evaluation operation, the word
line 14 is activated, as a result of which the memory
20   cells 15 connected to it can be read. The selection
transistors 45, 55 are initially switched in such a way
that the selection transistor MUX2 is switched on and
the selection transistor MUXEX2 is switched off (open),
with the result that the bit line pair 16 (the lower
25   two bit lines 12, 13) designated by "2" is coupled to
the first read/write amplifier element 40. Likewise,
the selection transistor MUX1 is switched off (open)
and the selection transistor MUXEX1 is switched on,
with the result that the upper bit line pair 16 (the
30   upper two bit lines 12, 13) designated by "1" is
coupled to the second read/write amplifier element 50.

The individual cell signals are initially amplified via
the bit lines 12, 13 by the second read/write amplifier
35   element 50 by means of the N latch circuit 51. As has
been thoroughly explained in the context of the general
description, this means that the voltage level of that
bit line 12 or 13 of a bit line pair which is lower by

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comparison of the two voltage values is amplified down
to the low level. This is because a uniform reference
voltage was applied to all the bit lines 12, 13 before
the beginning of the evaluation method.

5

The application of a uniform reference voltage value is
effected via the equalizer 43.

10   If the memory cells 15 to be read are activated, the
voltage value on the bit line 12 changes as a result of
this activation. The voltage value increases slightly,
for example, in the case of an information item logic
"1" stored in the memory cell 15, whereas the voltage
value decreases slightly, for example, in the case of
15   an information item logic "0". In the case of the
unactivated bit line, that is to say the reference bit
line   13,   however,   the   voltage   value   remains
substantially unchanged.

20   The N latch circuit 51 always amplifies down to a low
level that voltage value in a bit line pair 16 which
has the lower value in each case. If the voltage value
present on the bit line 12 is amplified down to a low
level, this means that the information in the memory
25   cell 15 to be evaluated was logic "0". If the voltage
value on the reference bit line 13 is amplified down to
a low level, this means that the information content in
the memory cell 15 to be evaluated was logic "1".

30   The cell signals are also amplified by the first
read/write amplifier element 40 at the same time as the
second read/write amplifier element 50. In this case,
the lower voltages are amplified to the low level by
means of the N latch circuit 41, while the respective
35   other cell signals are amplified to the full high level
by means of the P latch circuit 42. By way of example,
if the voltage signal of the bit line 12 to be
evaluated was pulled to a low level, the voltage value

of the reference bit line 13 is amplified to a high
level, or vice versa.

      After the writing back of the information items by the
 5   first read/write amplifier element 40, the bit line
      pairs 16 are disconnected by the selection transistors
      MUX1 or MUX2, with the result that they float at full
      voltage levels. The N latch circuit 41 of the first
      read/write amplifier element 30 is then switched off,
10   while the still active P latch circuit 42 is changed
      over to the bit line pair 16, connected to the second
      read/write   amplifier   element   50,   by   means   of
      corresponding driving of the selection transistors MUX1
      or MUX2. The N latch circuit 51 of the second
15   read/write amplifier element 50 is held active in this
      case. The voltages of the bit line pair 16 that have
      hitherto not been amplified can be amplified to full
      levels, that is to say to high levels, and written back
      to the memory cells 15.
20

      The requisite signal sequence of the sense amplifier
      driving is summarized in Figure 4. In this case V(EQ)
      denotes the voltage profile in the equalizer 43, V(WL)
      denotes the voltage profile in the word line 14,
25   V(MUX1EX) denotes the voltage profile in one of the
      selection transistors 55, V(MUX2EX) denotes the voltage
      profile of another selection transistor 55, V(MUX1)
      denotes the voltage profile of one selection transistor
      45, V(MUX2) denotes the voltage profile of another
30   selection transistor 45, V(NSETEX) denotes the voltage
      profile at the N latch circuit 51, V(NSET) denotes the
      voltage profile at the N latch circuit 41, and V(PSET)
      denotes the voltage profile at the P latch circuit 42.

35   Through activation of the bit switch 54, a voltage
      difference is generated on external data lines 31,
      which voltage difference can then be evaluated by the

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further read/write amplifier 32 and be amplified in a
suitable manner for further process steps.

The word line 14 is deactivated after the end of the
5   evaluation. By means of the equalizer 43, a uniform
reference voltage is once again set on all the bit
lines 12 and reference bit lines 13.

Figures 5a to 5c illustrate voltage profiles for the
10 internal read-out and writing back of information items
from/to bit line pair(s) 16 illustrated in Figure 3,
the respective bit line pairs 16 considered being
designated by a "1" and a "2".

15 Figure 5a illustrates the voltage profiles, in each
case the information item logic "0" being written to
the memory cells 15 to be evaluated in the
corresponding bit line pairs 16.

20 At the beginning of the evaluation method, a reference
voltage value is set on all the bit lines 12, 13, said
value being 0.75 volt in the present exemplary
embodiment. The cell signals of cell 1 and cell 2 are
then amplified by the N latch circuits 41, 51 of the
25 first 40 and second 50 read/write amplifier elements.
Since the information item logic "0" had originally
been written to both cells, the voltage value decreases
in the event of activation in comparison with the
reference voltage value, this being represented by the
30 slight fall at approximately 10 nsec in Figure 5a.
Since both voltage values on the bit lines 12 of the
memory cells to be evaluated are somewhat lower than
the respective reference voltage values, these voltage
values, designated by V(BL1) and V(BL2) in Figure 5a,
35 are pulled to a low potential by means of the N latch
circuits 41, 51, said low potential being 0 volts in
the present exemplary embodiment. Since the P latch
circuit 42 is also activated at the same time in the

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first read/write amplifier element 40, in this case the
higher voltage value of the reference bit line, said
value being designated as V(BBL2) in Figure 5a, is
amplified to the high level, which is 1.5 volts in the
5   exemplary embodiment. Since the second read/write
amplifier element 50 does not contain a P latch
circuit, the reference voltage value V(BBL1) is
initially present in a substantially unchanged form.

10   After the information items of the cells connected to
the first read/write amplifier element 40 have been
read out, evaluated and written back, the bit lines are
disconnected by the selection transistors, with the
result that they float at full voltage levels. The
15   selection transistors are then changed over in such a
way that the still active P latch circuit 42 of the
first read/write amplifier element 40 is connected to
the second read/write amplifier element 50, or to the
bit line pair connected thereto. In this case, the N
20   latch circuit 51 in the second read/write amplifier
element 50 is kept active, and the voltages that have
hitherto not been amplified, that is to say the
reference bit line voltage V(BBL1) in this case, can be
amplified to a full high level and subsequently be
25   written back to the cell. In the exemplary embodiment
in accordance with Figure 5a, this is done after a time
of approximately 50 nsec has elapsed. Once all the
cells have been evaluated, the word line 14 is
deactivated. By means of the equalizer 43, the
30   reference voltage of 0.75 volt is once again set on all
the bit lines, this being the case at approximately
70 nsec in the exemplary embodiment in accordance with
Figure 5a and being rendered apparent from the fact
that the individual voltage curves converge from the
35   respective full levels to the value of the reference
voltage.

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Figures 5b and 5c illustrate the voltage profiles for
other cell information constellations in each case.
Figure 5b considers a situation in which the
information item logic "1" had been written to the

5   first cell and the information item logic "0" had been
written to the second cell. Figure 5c illustrates a
case in which the information item logic "1" had in
each case been written to the two cells to be
evaluated. The profile of the respective voltage curves

10   ensues according to the rules described with regard to
Figure 5a. As can be seen from Figures 5b and 5c, the
voltage value of the bit line to be evaluated increases
in comparison with the reference voltage if the
information item logic "1" is written to the cell. This

15   then correspondingly affects the amplification of the
voltage levels in each case to the high level or to the
low level, the respective amplification being effected
according to the stipulations mentioned under Figure
5a.

20

Finally, Figures 6a and 6b illustrate the external
reading (Figure 6a) and the external writing (Figure
6b) of cell information items of a memory cell on the
bit line pair 16 designated by "1" in Figure 3. In the

25   case of reading, a voltage difference is generated by
the read/write amplifier element 50 after activation of
the bit switch 54 on the external data lines (MDQ and
BMDQ) 31, which voltage difference is identified by the
distance d rendered apparent by arrows in Figure 6a,

30   and can then be evaluated and suitably amplified by the
external second read/write amplifier 32.

In the case of writing in accordance with Figure 6b,
voltage levels are applied via the external data lines

35   (MDQ and BMDQ) 31 to the latch circuits of the
read/write amplifier elements, which enable these to
toggle in the respectively desired direction. Figure 6b
illustrates how, on the bit line pair 1 (see Figure 3),

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the cell information item logic "0" is overwritten with
an information item logic "1".

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